Thermal Test Chip for Thermal Characterization and Qualification of Materials and Semiconductor Packages

Speaker: Mohamad Abo Ras - Berliner Nanotest und Design GmbH, Berlin, Germany

Email: aboras@nanotest.eu

Abstract

This work presents a novel thermal test chip (TTC) designed for thermal characterization, reliability investigation, and monitoring of semiconductor packages, thermal materials, and package materials.

The TTC is designed as a modular die with the smallest full functional die cell of 3.2mm x 3.2mm, consisting of heater structure and a temperature sensor. Figure 1 (below) illustrates the layout of a single cell (left) and 3x3 cell matrix (right).

The TTC can be used in any desired matrix, such as square or rectangular. All temperature sensors, whether in a single cell or an arrayed cell configuration, can be addressed individually to allow highly localized temperature measurement. Heating resistors on each die cell can be powered individually in serial or parallel configuration, highly useful for characterization of specific applications to mimic different electrical resistance values, hot spots, and heat fluxes.

Two types have been developed. One is intended for flip-chip die with a pure silicon backside. The second is intended for wire bond packages with gold backside metallization. Unique design challenges for these TTCs included design of the heater structure and temperature sensor with only a single titanium layer as adhesion and barrier layer.

These thermal test die can be used for applications such as : - Characterization of thermal interface materials (TIMs) under real conditions, as the TIM can be tested between silicon and metal surfaces.